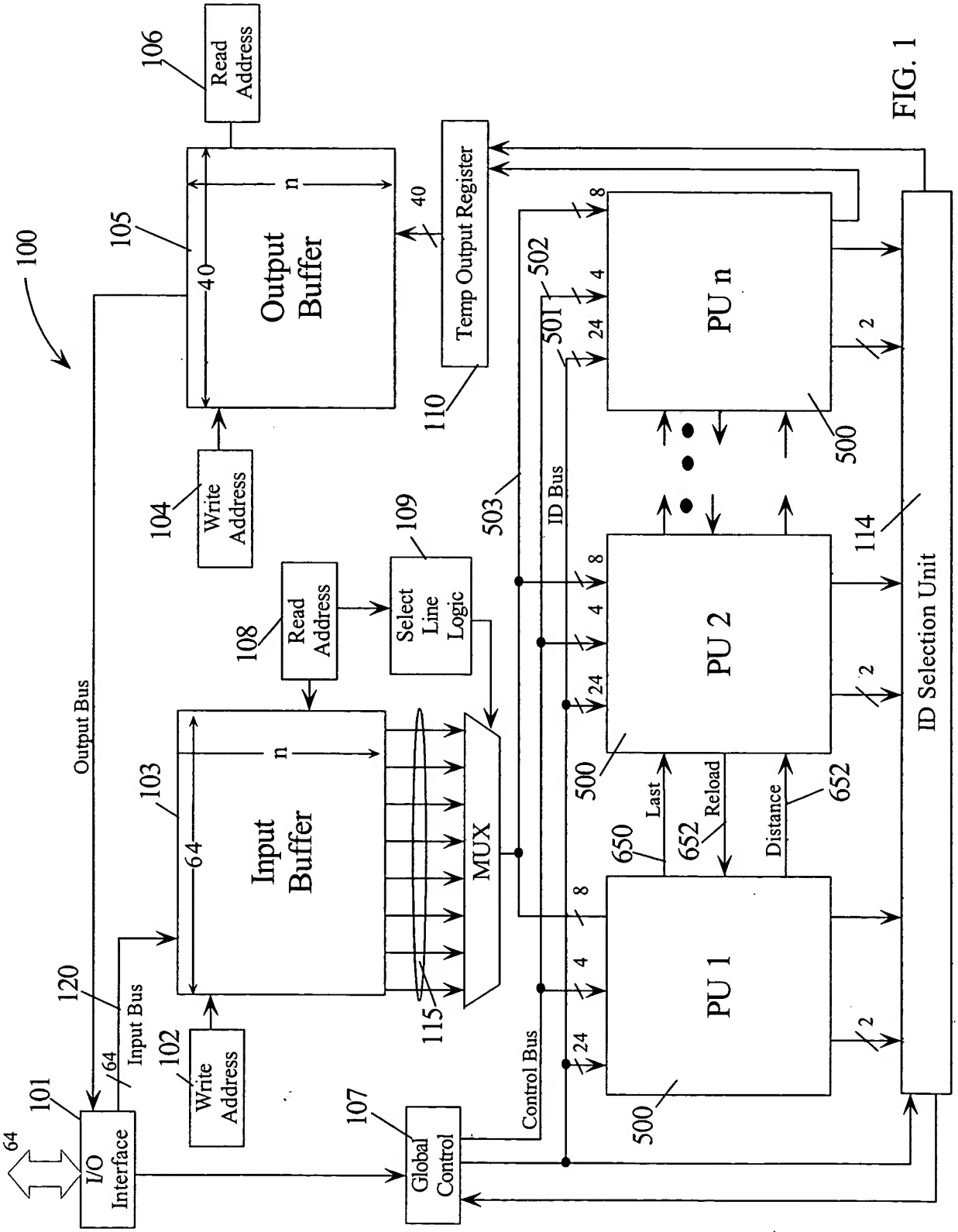

100
101
I/O Interface
64
120
Input Bus
64
102
Write Address
103
Input Buffer
n
64
Output Bus
105
Output Buffer
n
40
106
Read Address
104
Write Address
107
Global Control
108
Read Address
109
Select Line Logic
110
Temp Output Register
40
115
MUX
Control Bus
ID Bus
501
502
503
500
PU 1
PU 2
PU n
8
4
24
2
650
652
Last
Reload
Distance
652
114
ID Selection Unit

FIG. 1

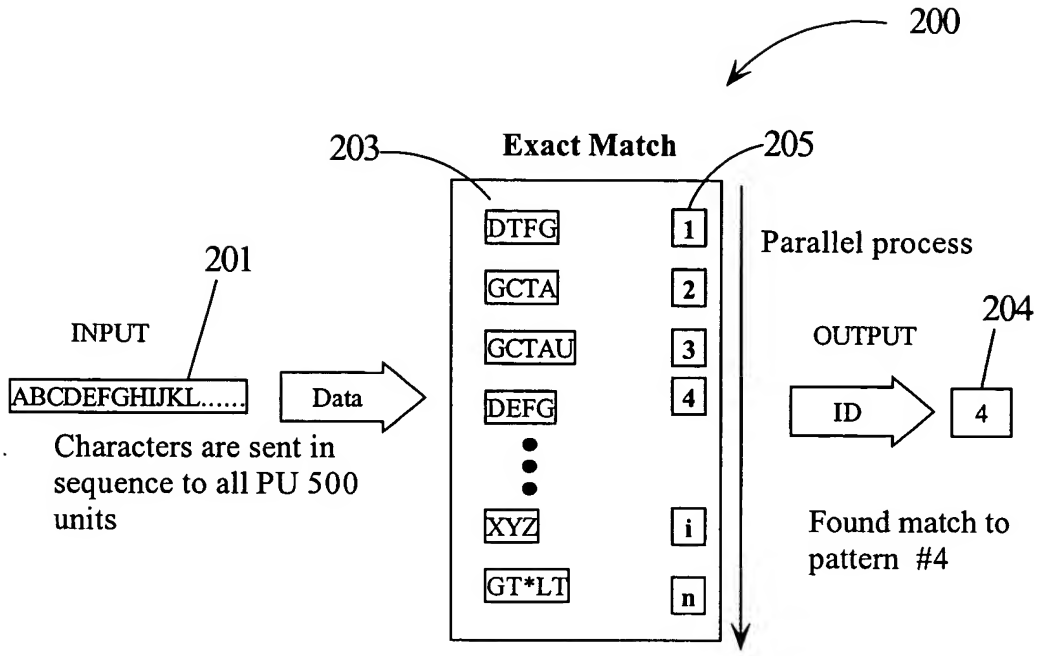

200
203
Exact Match
205
DTFG
GCTA
GCTAU
DEFG
XYZ
GT*LT
1
2
3
4
i
n
Parallel process
201
INPUT
ABCDEFGHIJKL.....
Data
Characters are sent in sequence to all PU 500 units
OUTPUT
204
ID
4
Found match to pattern #4

FIG 2A

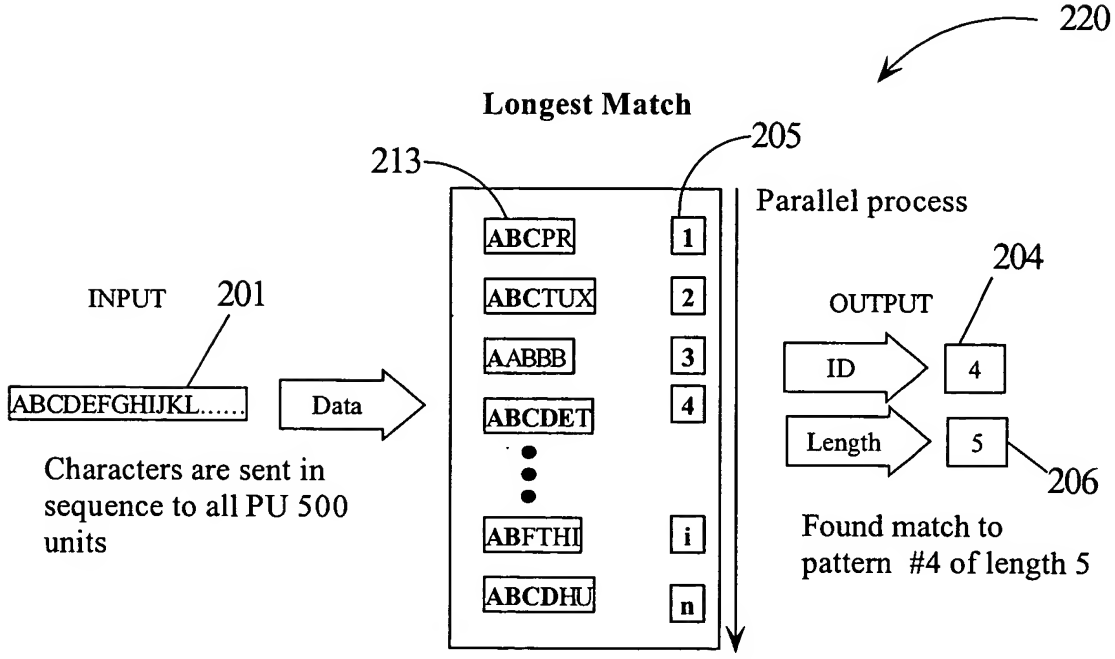

220
Longest Match
213
205
ABCPR
ABCTUX
AABBB
ABCDET
ABFTHI
ABCDHU
1
2
3
4
i
n
Parallel process
INPUT
201
ABCDEFGHIJKL.....
Data
Characters are sent in sequence to all PU 500 units
204
OUTPUT
ID
4
Length
5
206
Found match to pattern #4 of length 5

FIG 2B

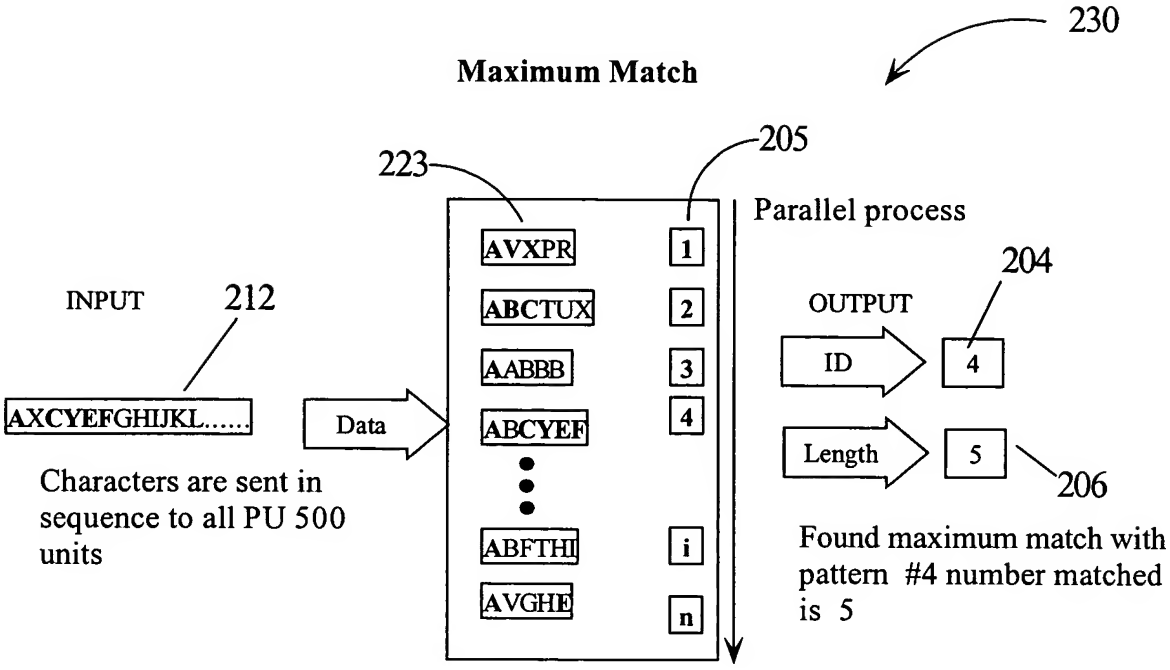

230
Maximum Match
205
223
Parallel process
AVXPR
ABCTUX
AABBB
ABCYEF
ABFTHI
AVGHE
1
2
3
4
i
n
INPUT
212
AXCYEFGHIJKL.....
Data
Characters are sent in sequence to all PU 500 units
OUTPUT
204
ID
4
Length
5
206
Found maximum match with pattern #4 number matched is 5

FIG 2C

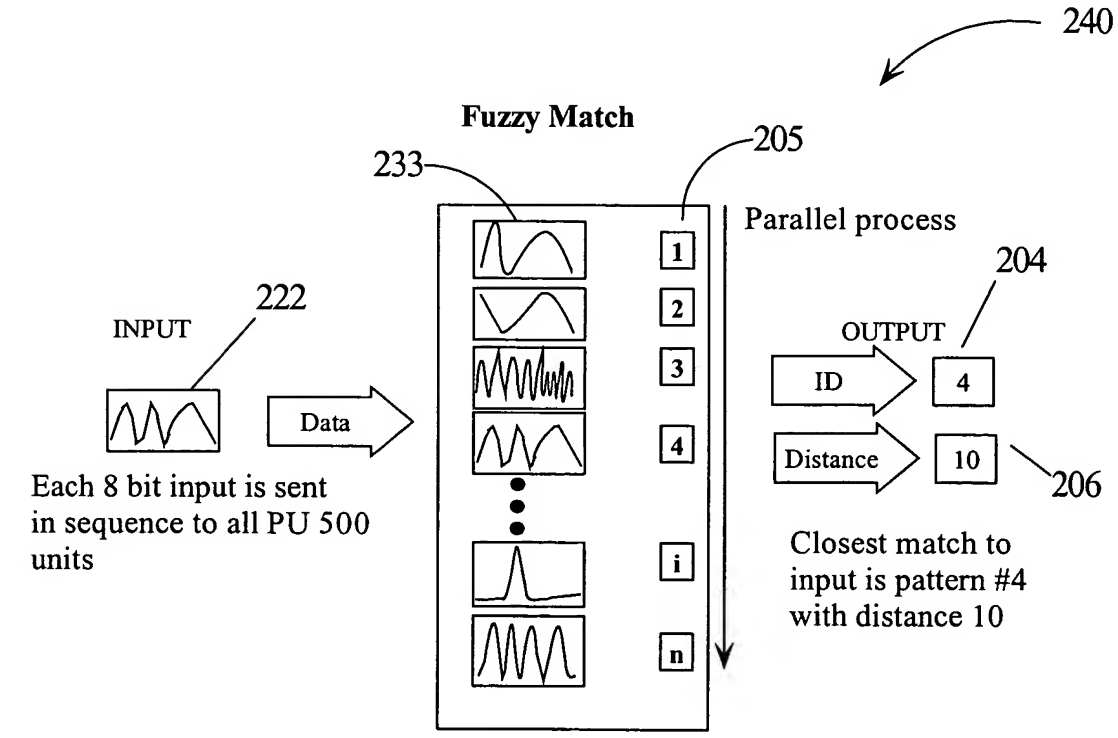

240
Fuzzy Match
205
233
Parallel process
1
2
3
4
i
n
INPUT
222
Data
Each 8 bit input is sent in sequence to all PU 500 units
OUTPUT
204
ID
4
Distance
10
206
Closest match to input is pattern #4 with distance 10

FIG 2D

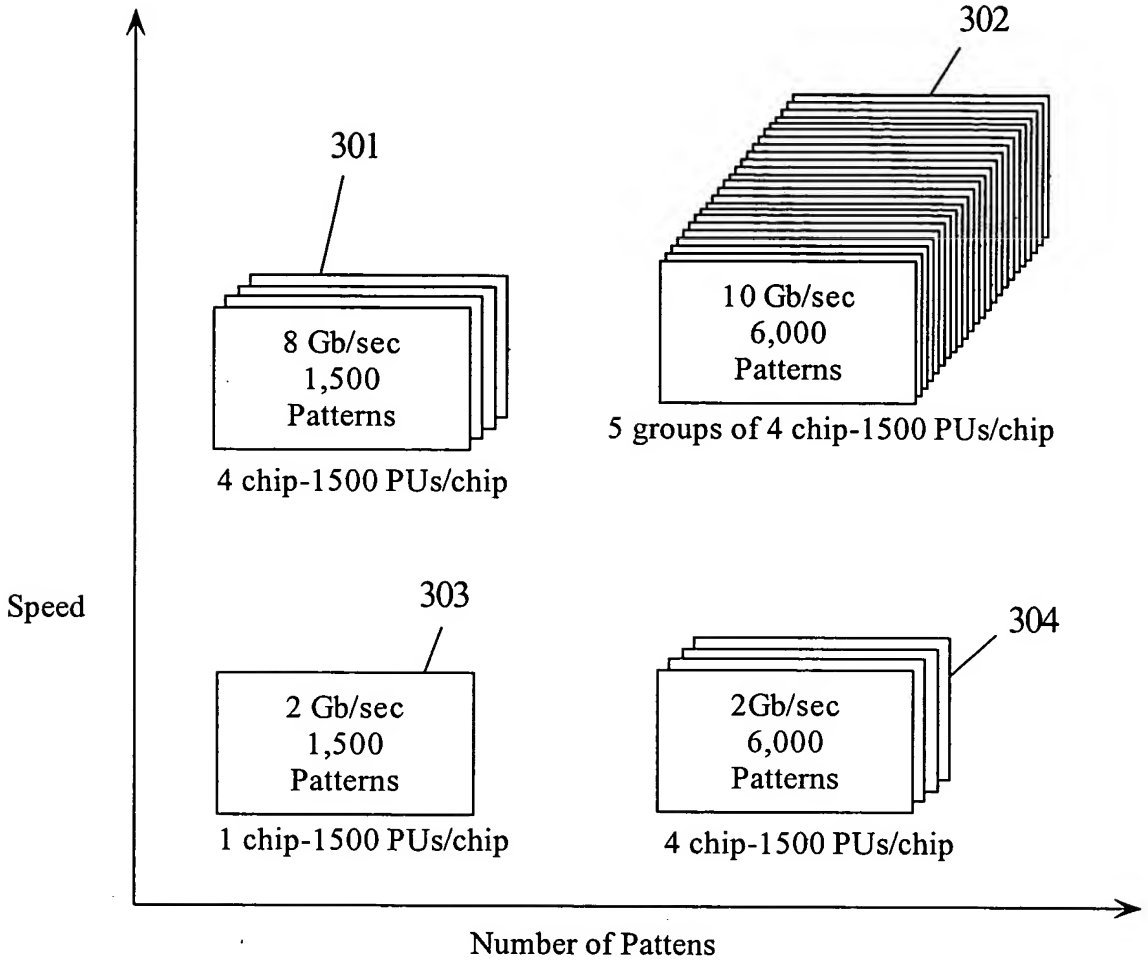

302
301
8 Gb/sec
1,500
Patterns
10 Gb/sec
6,000
Patterns
4 chip-1500 PUs/chip
5 groups of 4 chip-1500 PUs/chip
Speed
303
304
2 Gb/sec
1,500
Patterns
2Gb/sec
6,000
Patterns
1 chip-1500 PUs/chip
4 chip-1500 PUs/chip
Number of Pattens

FIG. 3

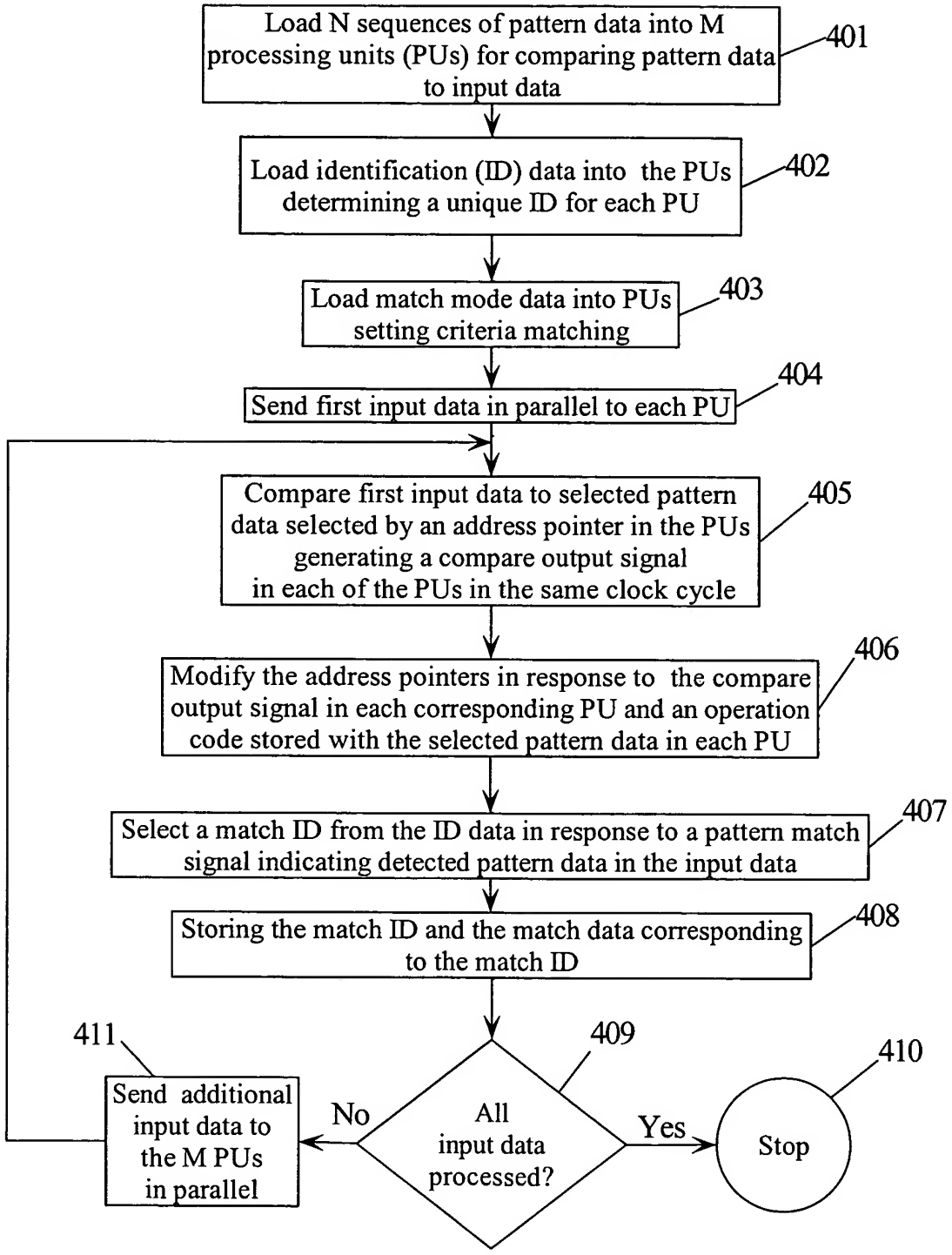

Load N sequences of pattern data into M processing units (PUs) for comparing pattern data to input data
401
Load identification (ID) data into the PUs determining a unique ID for each PU
402
Load match mode data into PUs setting criteria matching
403
Send first input data in parallel to each PU
404
Compare first input data to selected pattern data selected by an address pointer in the PUs generating a compare output signal in each of the PUs in the same clock cycle
405
Modify the address pointers in response to the compare output signal in each corresponding PU and an operation code stored with the selected pattern data in each PU
406
Select a match ID from the ID data in response to a pattern match signal indicating detected pattern data in the input data
407
Storing the match ID and the match data corresponding to the match ID
408
All input data processed?
409
No
Yes
Stop
410
Send additional input data to the M PUs in parallel
411

FIG. 4

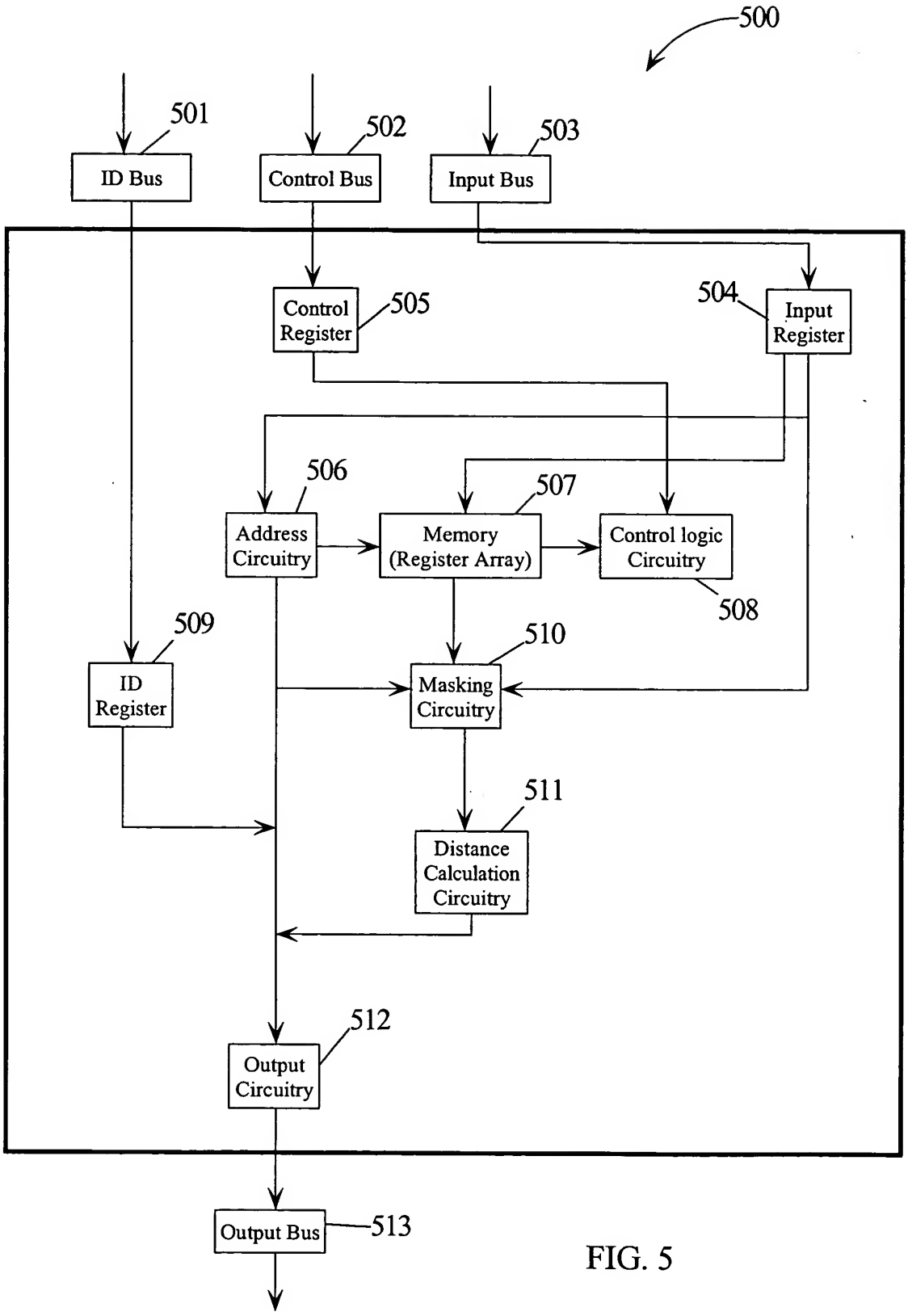

500
501
ID Bus
502
Control Bus
503
Input Bus
Control Register
505
504
Input Register
506
Address Circuitry
507
Memory (Register Array)
Control logic Circuitry
508
509
ID Register
510
Masking Circuitry
511
Distance Calculation Circuitry
512
Output Circuitry
Output Bus
513

FIG. 5

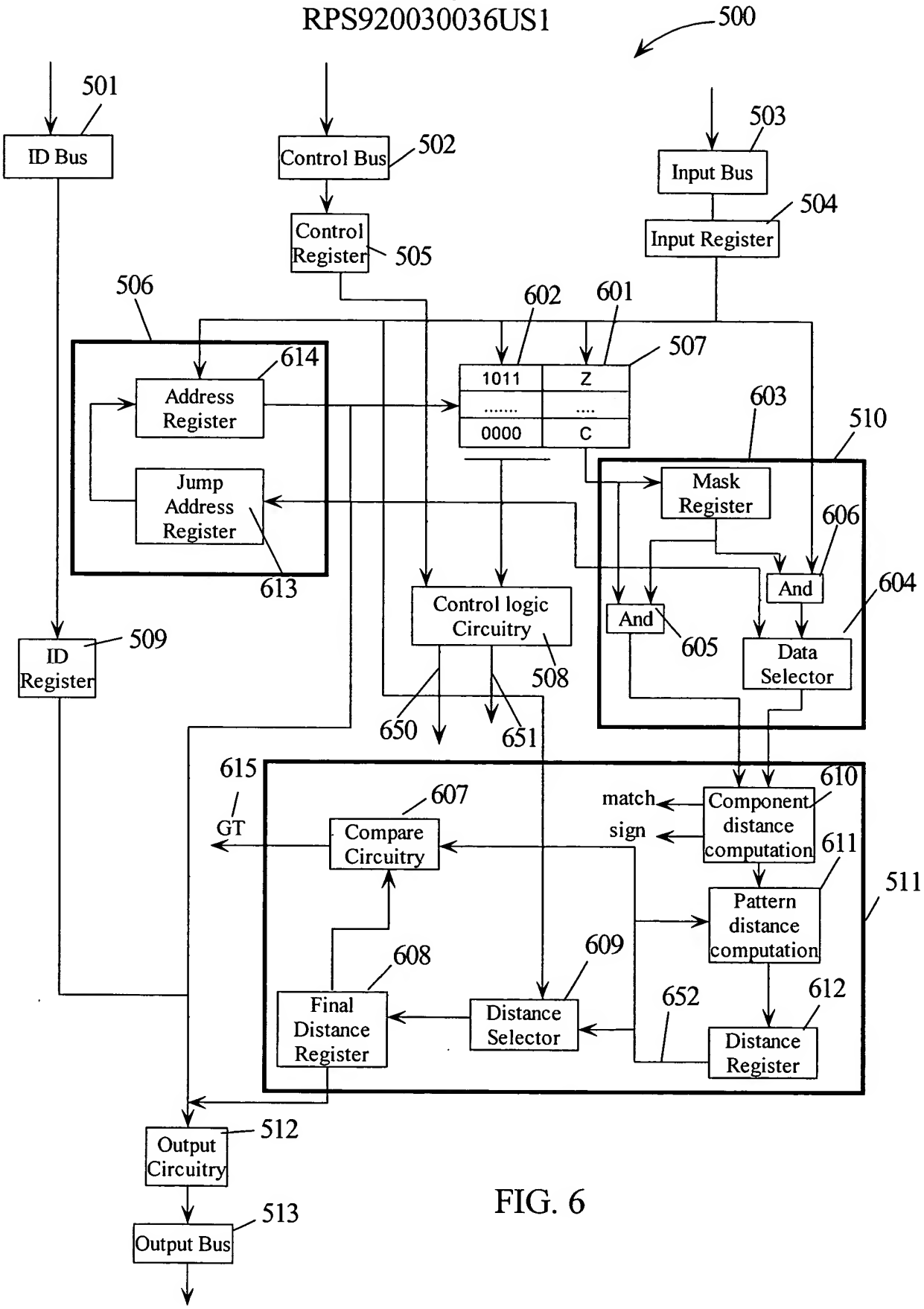

500
501
ID Bus
Control Bus
502
503
Input Bus
504
Input Register
Control Register
505
506
602
601
507
614
Address Register
1011
Z
.....
....
0000
C
603
510
Mask Register
606
Jump Address Register
613
And
604
Control logic Circuitry
And
605
ID Register
509
Data Selector
508
650
651
615
610
607
match
GT
Compare Circuitry
sign
Component distance computation
611
511
Pattern distance computation
608
609
652
612
Final Distance Register
Distance Selector
Distance Register
512
Output Circuitry
513
Output Bus

FIG. 6

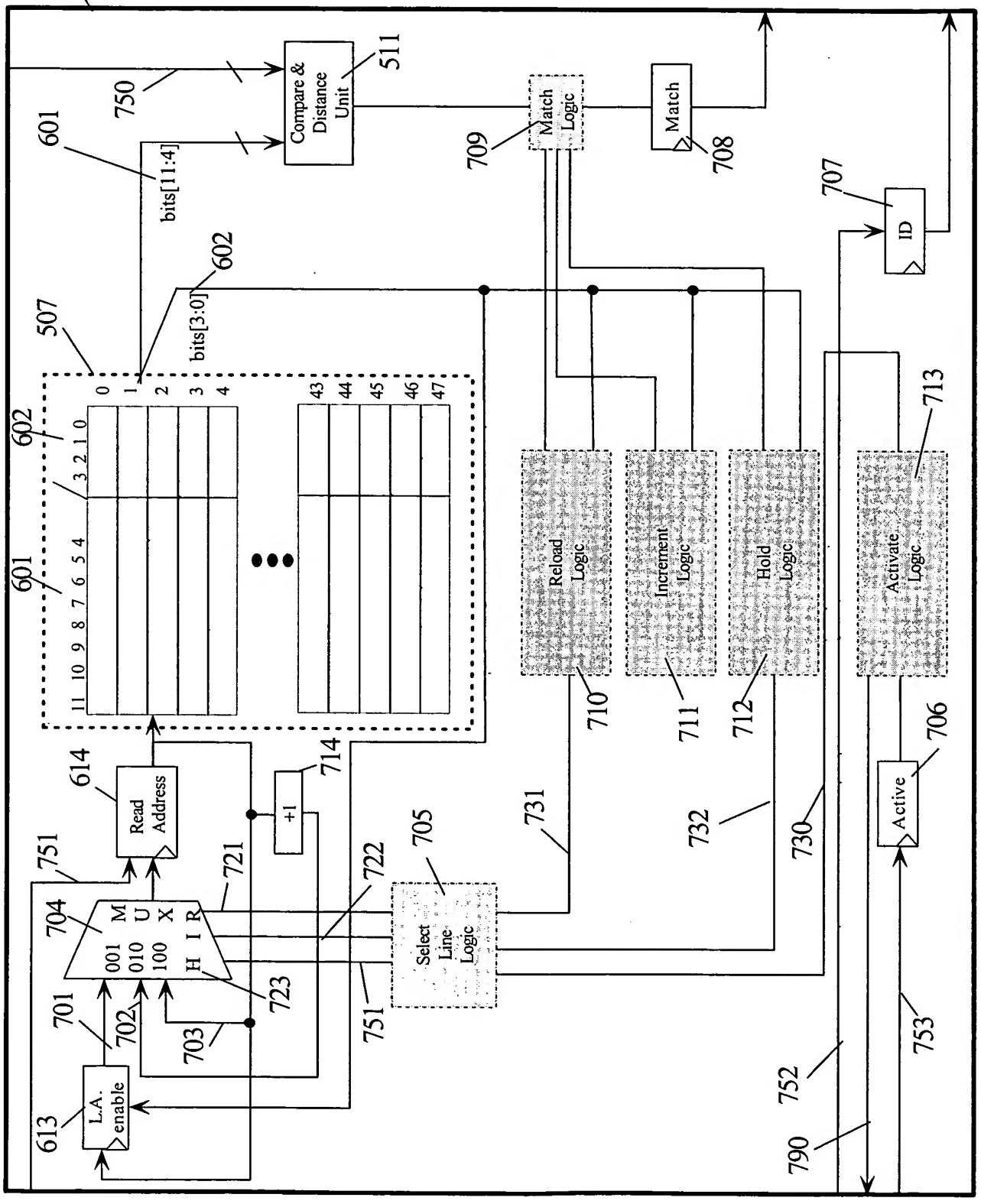
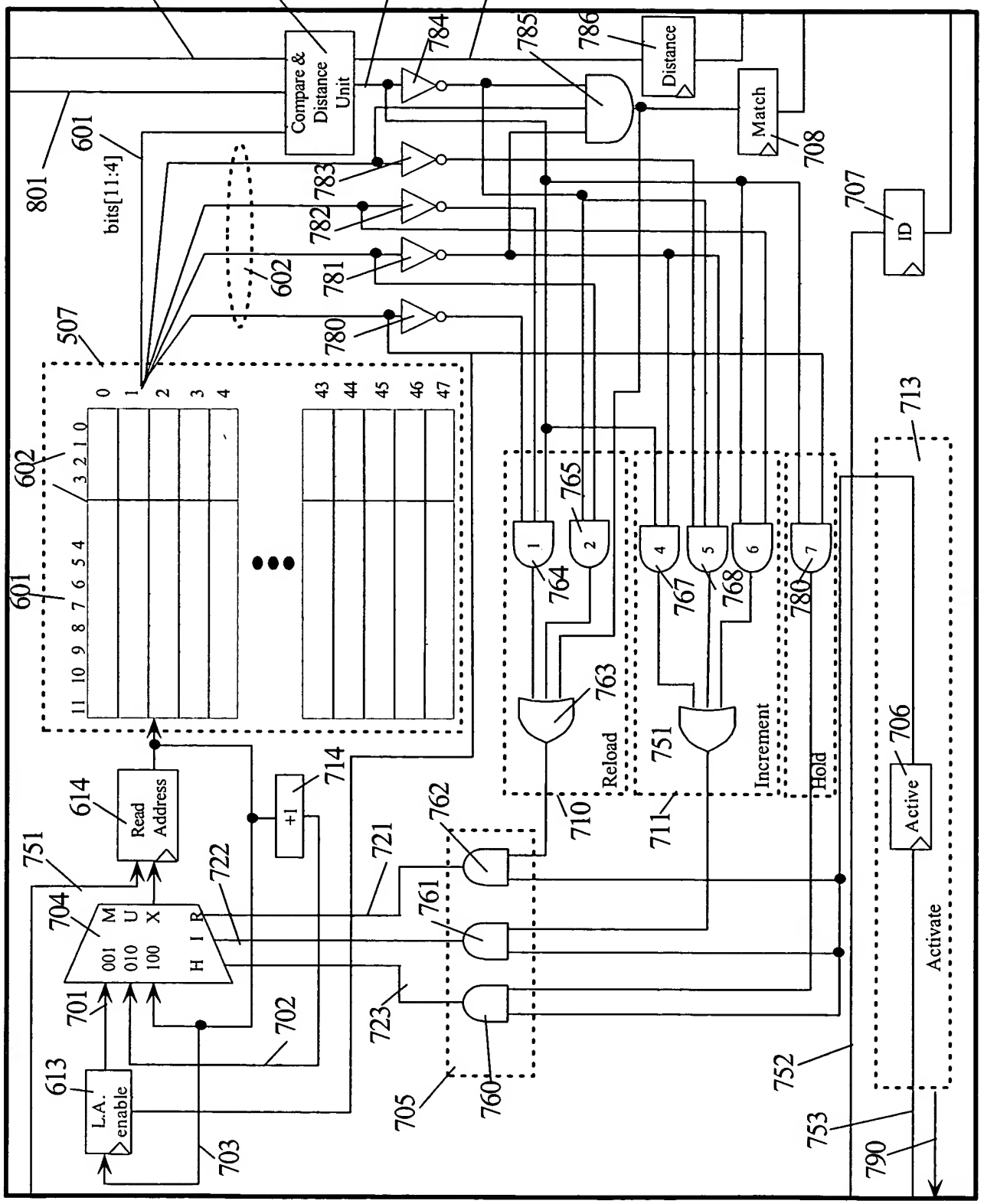

500
Compare & Distance Unit
511
750
601
bits[11:4]
602
bits[3:0]
507
Match Logic
709
Match
708
707
ID
Reload Logic
710
Increment Logic
711
Hold Logic
712
Activate Logic
713
Read Address
614
+1
714
705
731
732
730
Active
706
704
MUX
001
010
100
HIR
721
722
723
751
Select Line Logic
701
702
703
L.A. enable
613
752
753
790

FIG. 7

FIG. 8


750
511
771
772
784
785
786
Distance
Compare & Distance Unit
Match
708
801
601
bits[11:4]
783
782
781
780
602
507
707
ID
0 1 2 3 4
43 44 45 46 47
11 10 9 8 7 6 5 4 3 2 1 0
765
764
767
768
780
763
713
Reload
Increment
Hold
710
711
751
706
Active
Activate
614
Read Address
714
+1
762
721
722
761
704
M U X
001 010 100
H I R
701
702
723
705
760
752
753
790
613
L.A. enable
703

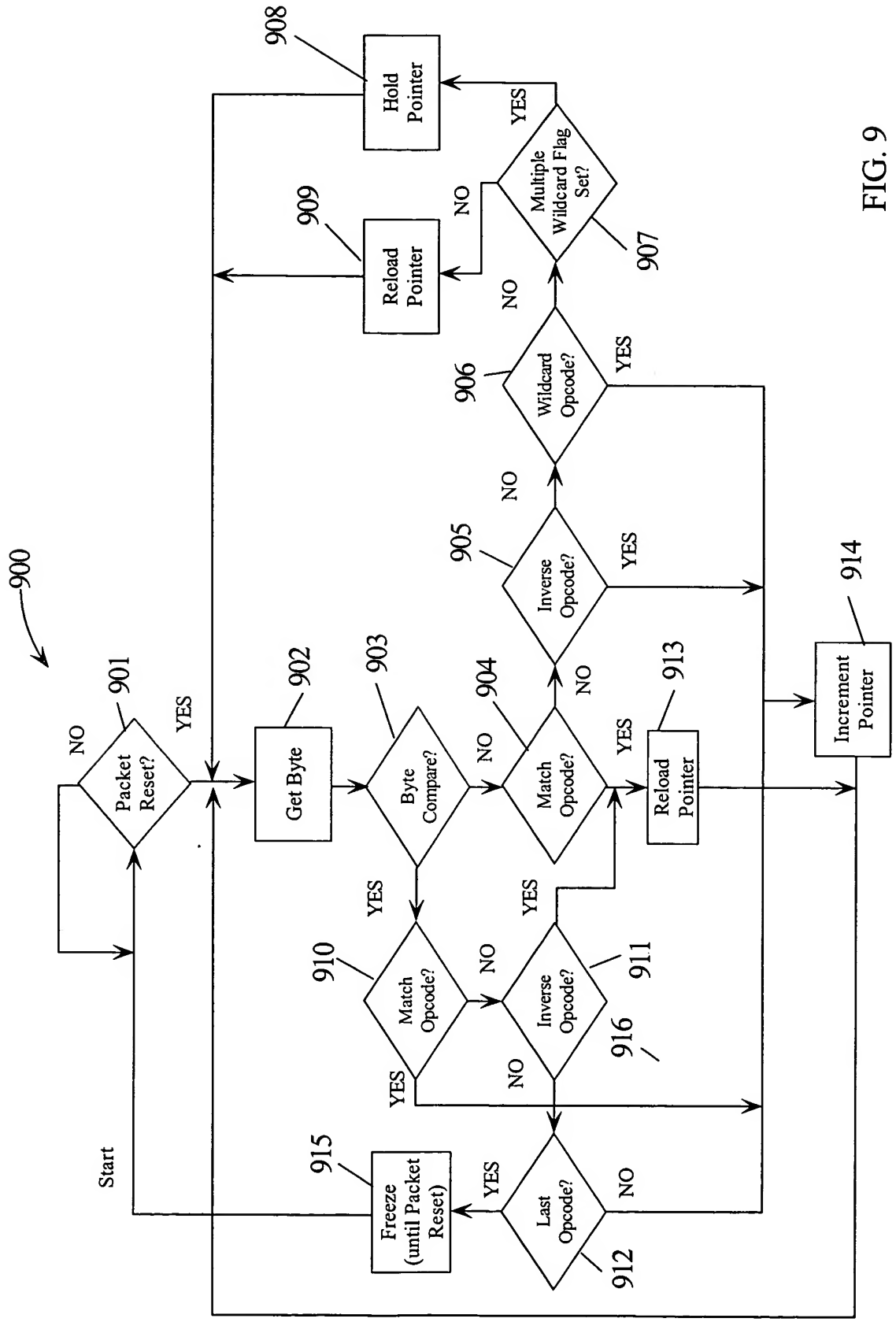

900
Start
Packet Reset?
901
NO
YES
Get Byte
902
Byte Compare?
903
NO
YES
Match Opcode?
904
NO
YES
Inverse Opcode?
905
NO
YES
Wildcard Opcode?
906
NO
YES
Multiple Wildcard Flag Set?
907
NO
YES
Hold Pointer
908
Reload Pointer
909
Match Opcode?
910
NO
YES
Inverse Opcode?
911
NO
YES
Last Opcode?
912
NO
YES
Reload Pointer
913
Increment Pointer
914
Freeze (until Packet Reset)
915
916

FIG. 9

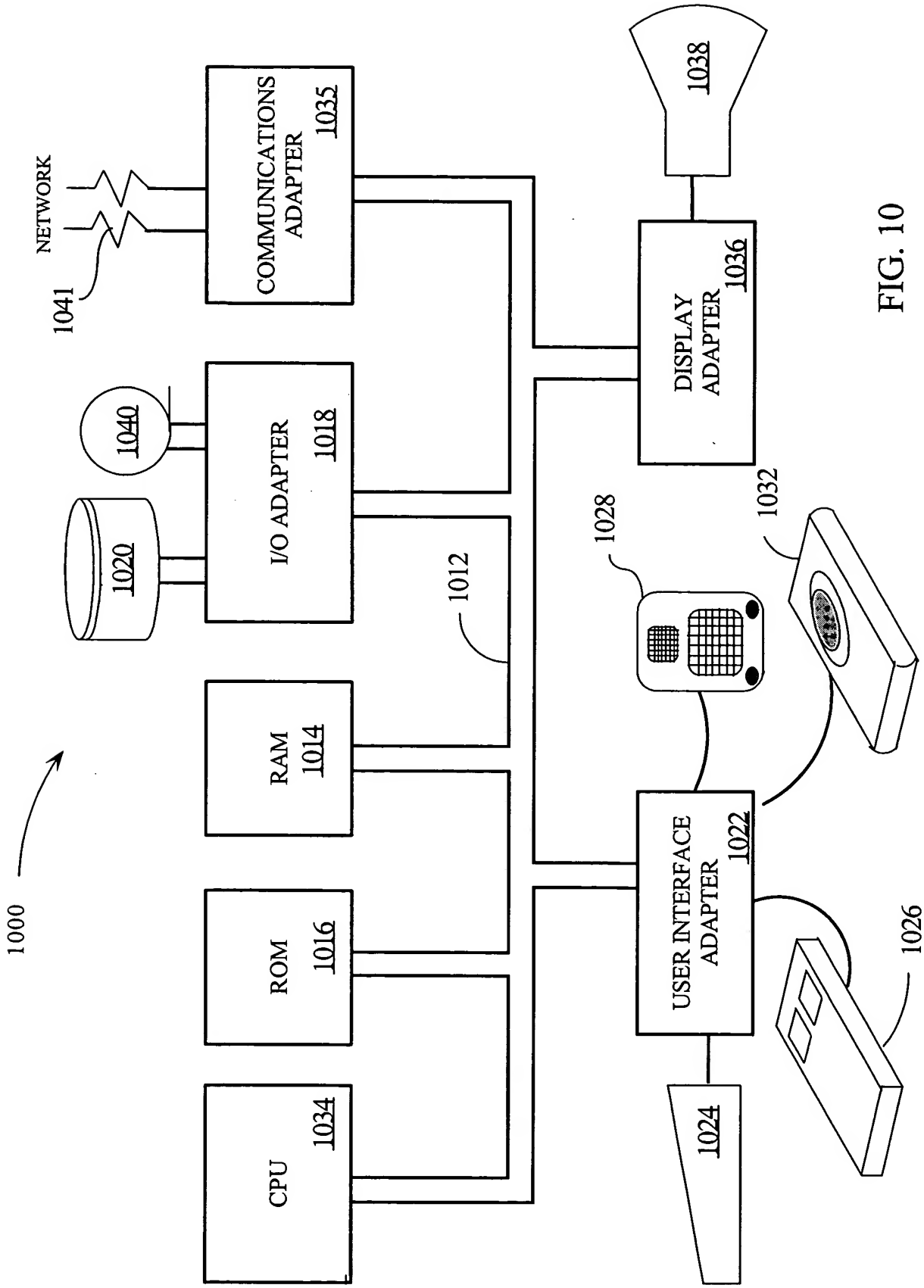

1000
CPU 1034
ROM 1016
RAM 1014
1012
I/O ADAPTER 1018
1020
1040
NETWORK
1041
COMMUNICATIONS ADAPTER 1035
1038
DISPLAY ADAPTER 1036
1028
1032
USER INTERFACE ADAPTER 1022
1024
1026

FIG. 10

Case 1: Reload if there is NOT a pattern match and the match OPcode is set
Partial expression to match: "ABC"

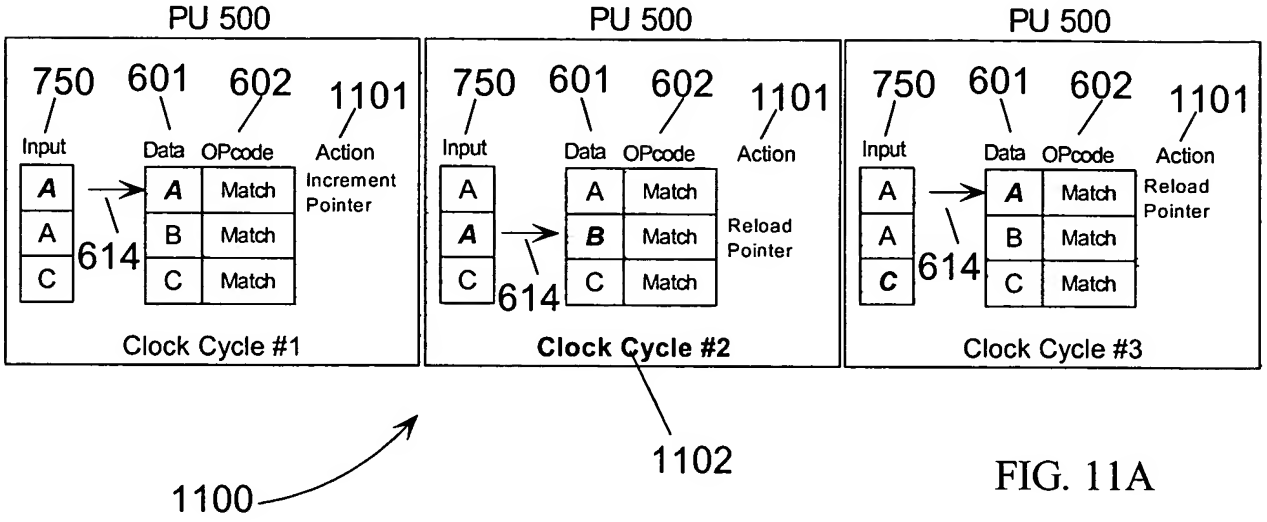


FIG. 11A

Case 2: Reload if there is a pattern match and the inverse OPcode is set for a pattern byte
Partial Expression to match : "C!DE"

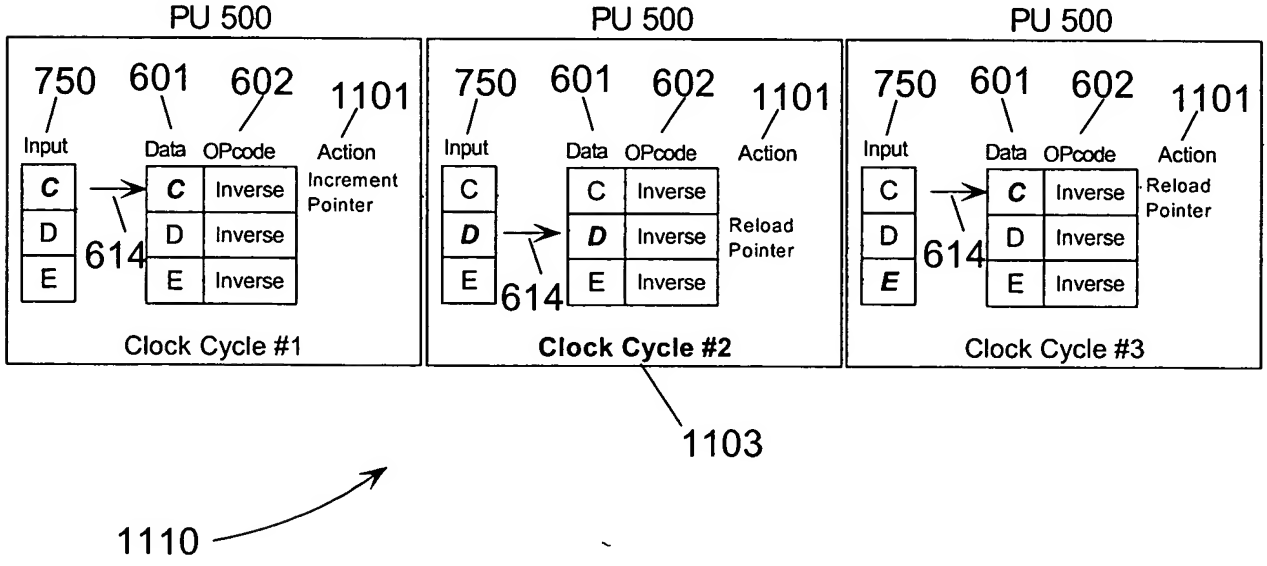


FIG. 11B

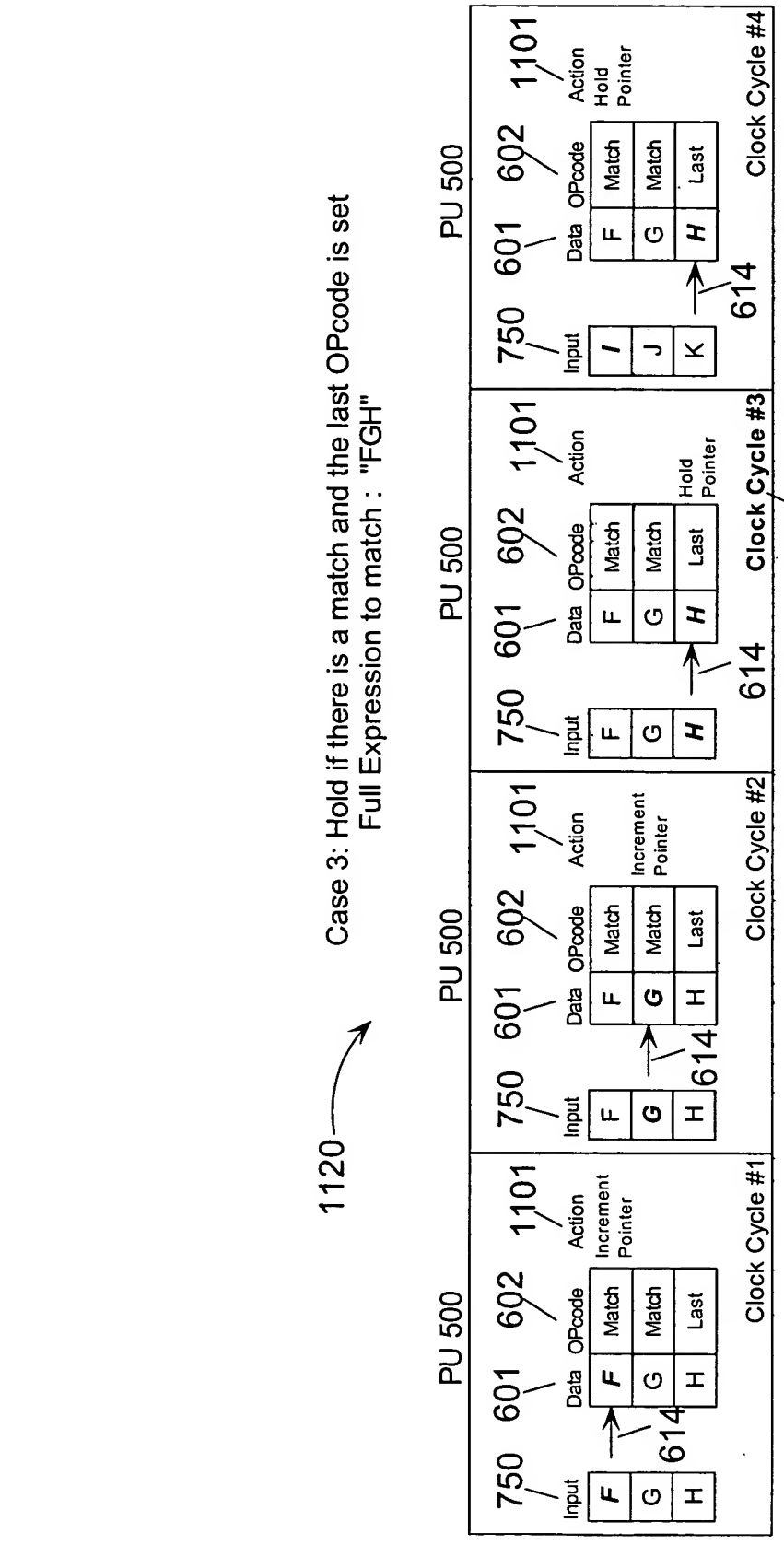

Case 3: Hold if there is a match and the last OPcode is set
Full Expression to match : "FGH"
1120
PU 500
Clock Cycle #1
Clock Cycle #2
Clock Cycle #3
Clock Cycle #4
1104
Input
Data
OPcode
Action
Increment Pointer
Hold Pointer
Match
Last
614

FIG. 11C

Case 4: Increment if there is NOT a pattern match and the inverse OPcode is set
Partial expression to match: "I!LK"

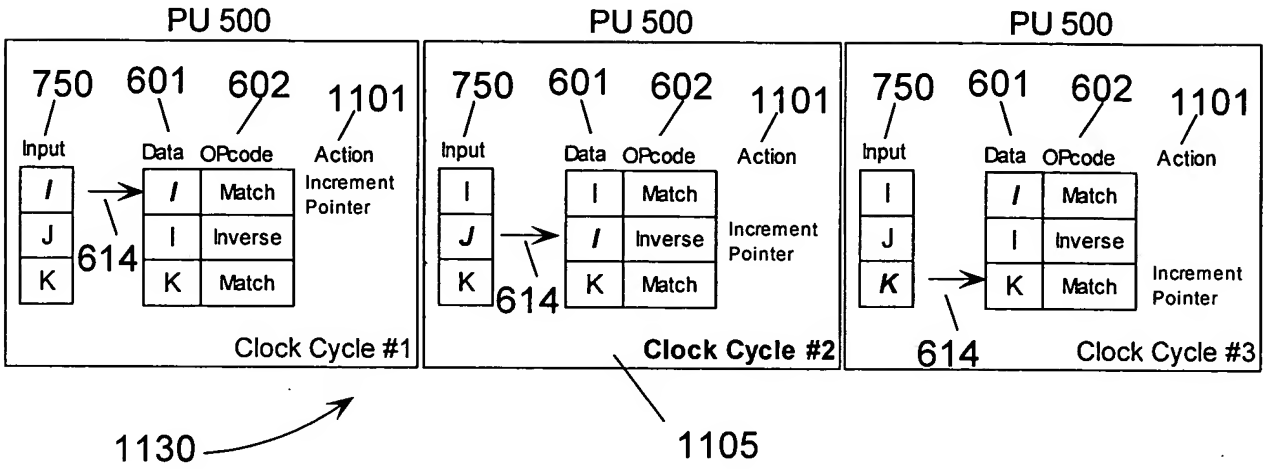


FIG. 11D

Case 5: Increment if there is a pattern match and the match OPcode is set
Partial Expression to match : "LMN"

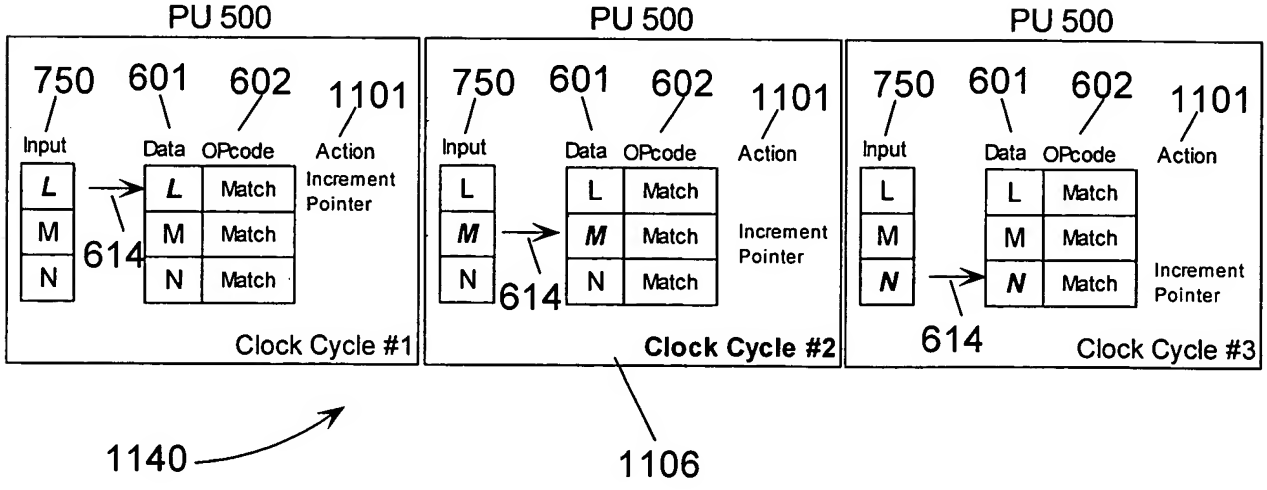


FIG. 11E

Case 6: Increment if there is NOT a pattern match and the wildcard OPcode is set
Partial expression to match: "O•Q"

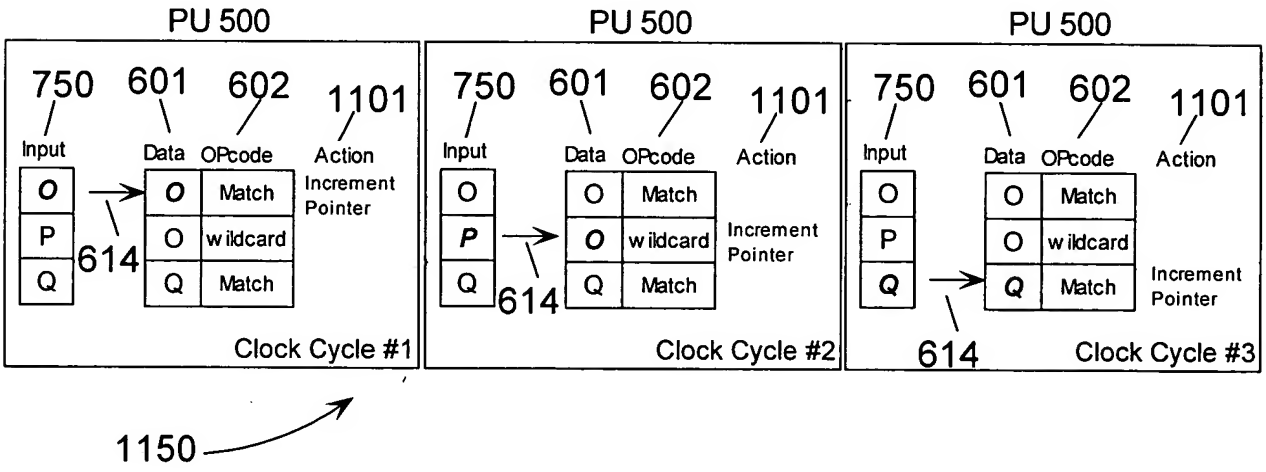


FIG. 11F

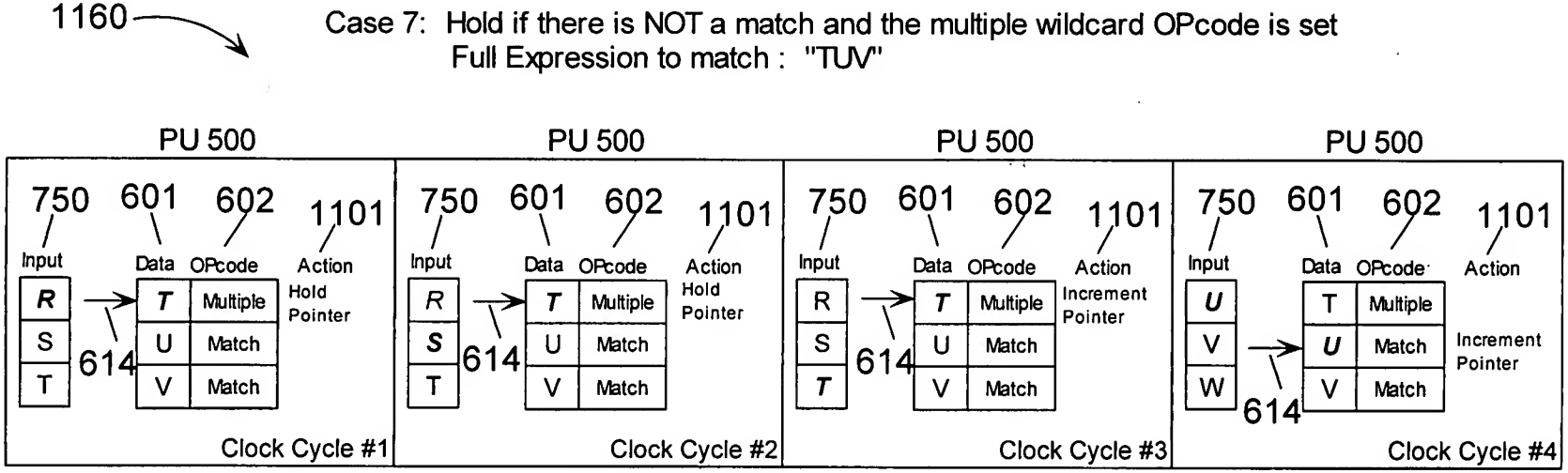

1160
Case 7: Hold if there is NOT a match and the multiple wildcard OPcode is set
Full Expression to match : "TUV"
PU 500
PU 500
PU 500
PU 500
750
601
602
1101
Input
Data
OPcode
Action
Hold Pointer
Increment Pointer
R
S
T
U
V
W
Multiple
Match
614
Clock Cycle #1
Clock Cycle #2
Clock Cycle #3
Clock Cycle #4

FIG. 11G

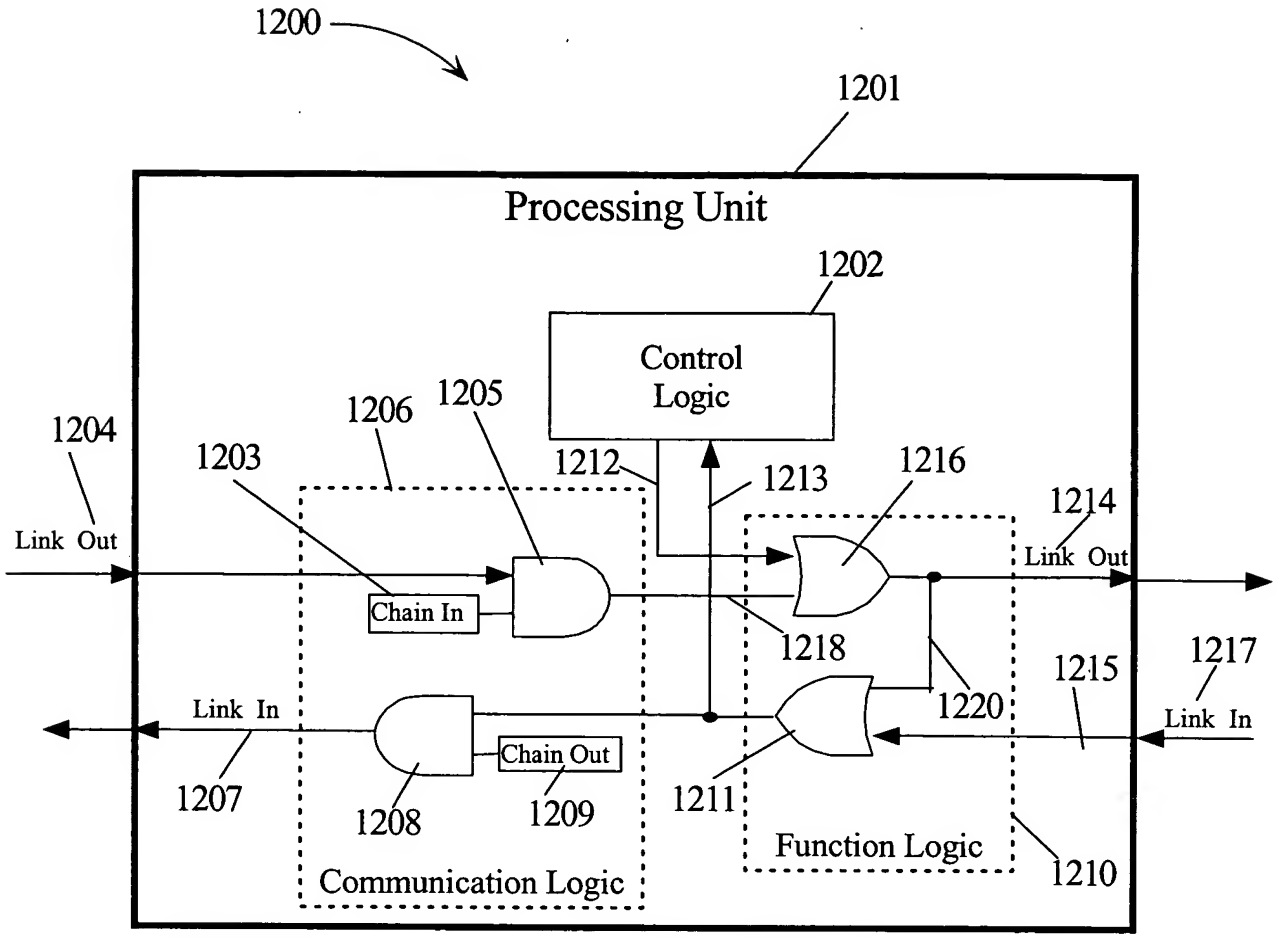

1200
1201
Processing Unit
1202
Control Logic
1204
Link Out
1203
1206
1205
1212
1213
1216
1214
Link Out
Chain In
1218
1217
1215
Link In
1220
Link In
1207
Chain Out
1208
1209
1211
Function Logic
1210
Communication Logic

FIG. 12

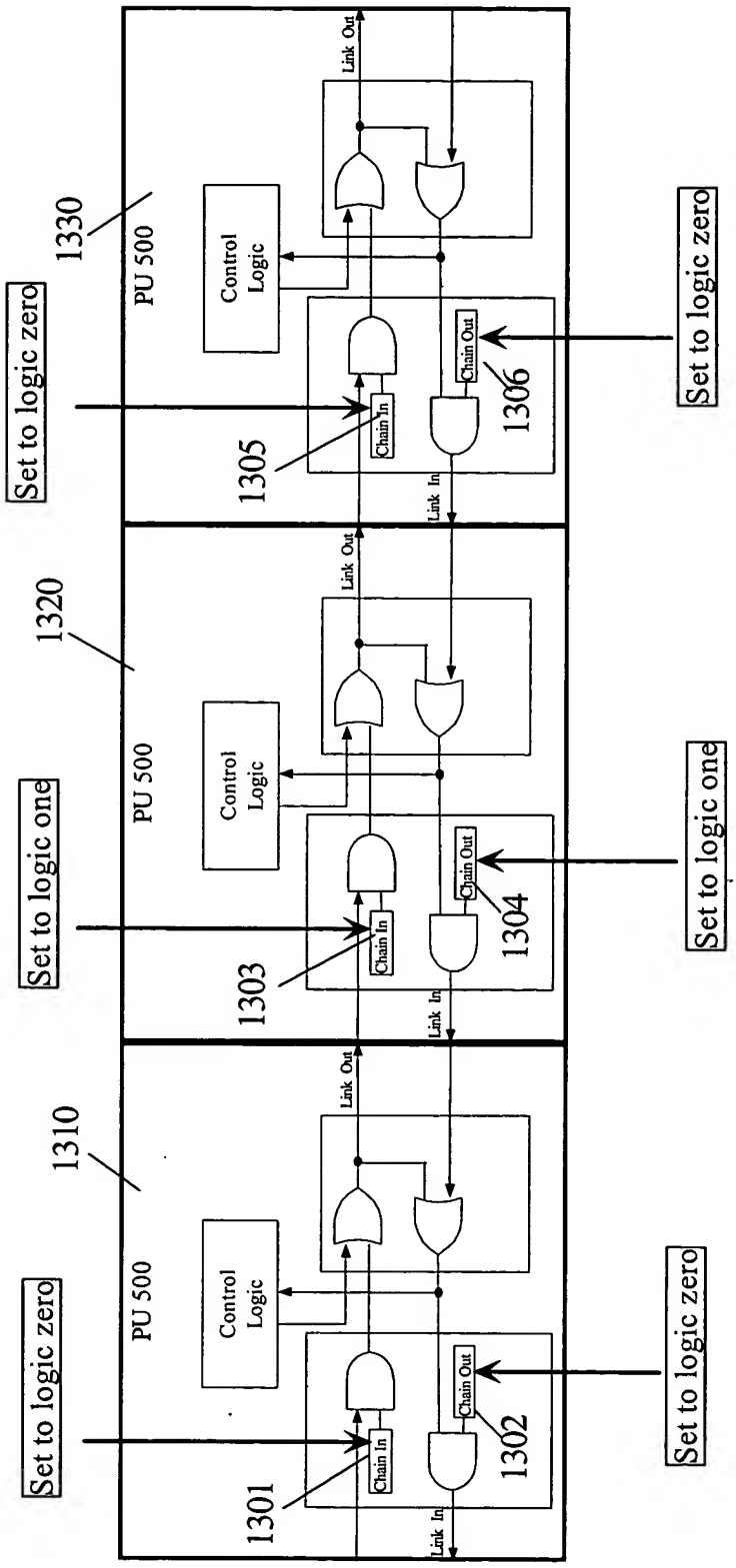

1330
PU 500
Control Logic
Link Out
Chain In
Chain Out
Link In
Set to logic zero
1305
1306
Set to logic zero
1320
PU 500
Control Logic
Link Out
Chain In
Chain Out
Link In
Set to logic one
1303
1304
Set to logic one
1310
PU 500
Control Logic
Link Out
Chain In
Chain Out
Link In
Set to logic zero
1301
1302
Set to logic zero

FIG. 13